Amendments to the Specification:

Please replace paragraph [0051] with the following amended paragraph:

[0051] In one embodiment, puncture biasing for parity bits P1 and P2 is implemented for one stage rate matching. Figure 10 is a schematic block diagram showing circuitry 600 for 3GPP rate matching for HSDPA, using a Turbo coded HS-DSCH. The circuitry 600 implements a 3GPP rate-matching scheme for HSDPA. The circuitry 600 includes a bit separation circuit 605, a first rate matching stage 610, a virtual incremental redundancy (IR) buffer 615, a second rate matching stage 620 and a bit collection circuit 625. The first rate matching stage ~~605~~ 610 includes a Parity 1 (P1) bit rate matching circuit 630 and Parity 2 (P2) bit rate matching circuit 635. The second rate matching stage 620 includes a systematic ~~bits~~ bit rate matching circuit 640, a Parity 1 (P1) bit rate matching circuit 645 for the second rate matching and a Parity 2 (P2) bit rate matching circuit 650 for the second rate matching. In operation, the systematic bits, Parity 1 (P1) and Parity 2 (P2) bits are processed through the first rate matching stage 610, virtual IR buffer 615, second rate matching stage 620 and bit collection circuit 625. Note that the Parity 1 (P1) and Parity 2 (P2) bits are treated separately. The systematic bits, Parity 1 (P1) and Parity 2 (P2) bits are combined at the bit collection circuit 625 to provide a single data output N_{data}. Also note that if the number of coded bits is less than or equal to the size of the virtual IR buffer 615, the first ~~stage of~~ rate matching stage 630 is transparent. The transparent first stage case and Rel-4 rate matching are considered.

Please replace paragraph [0053] with the following amended paragraph:

[0053] The rate matching algorithm performs puncturing if the overall code rate is greater than 1/3 and repetition if the code rate is less than 1/3. Currently code rates greater than 1/3 are accomplished by applying the same puncturing rate to both P1 and P2 bits (to within one bit) but with different puncturing pattern phases. In order to avoid non-puncturing periodicities that have been shown to degrade the Turbo code performance, the puncturing rates for P1 and P2 be independently biased. For example, if the number of P1 bits is decreased by $\underline{\Delta}$ and the number of P2 bits is increased by $\underline{\Delta}$, the overall code rate is unchanged but the problematic non-puncturing periods can be avoided. Given this approach to avoiding the problematic code rates, an analytical expression for the requisite bias, has been derived.